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1. 概要(Summary)

Modern-day electronics are close to the limit of miniaturization following Moore's law. New device architectures such as JLTs and SETs are being suggested. As this CMOS technology continues to advance, it has been extended from micrometer to nanometer scale, hence the existence of nanofabrication. Using nanotechnology, the narrowest line pattern can possible through the EB lithography process. This paper presents the design, fabrication, and electrical characterization of MOSFETs, CMOS inverter, and n-doped and co-doped Junctionless transistors(JLTs).

2. 実験(Experimental)

【利用した主な装置】

ﾚｲｱｳﾄ設計ﾂｰﾙ、酸化炉、ﾏｽｸﾚｽ露光装置、ｲｵﾝ注入装置、ｳｪﾙ拡散炉、Al ｽﾊﾟｯﾀ装置、ｴｯﾁﾝｸﾞ装置(ﾚｼﾞｽﾄ Ashing 用)、PMA 炉、ﾃﾞﾊﾞｲｽ測定. nMOS, pMOS, CMOS inverter, n-doped junctionless transistor, and Co-doped junctionless transistors were fabricated by using the above experimental procedure.

3. 結果と考察(Results and Discussion)

To understand the device behavior, electrical measurements were carried out at the temperatures 8.3 K and 300 K. Drain current I_D *vs* gate voltage V_G characteristics were measured for different V_{DS} and substrate set to the ground. Fig. 1, and 2 represents the nMOS and pMOSFET characteristics. Electrical characteristics of CMOS inverter has been shown in Fig. 3. It consists of nMOS and pMOSFET. When high Voltage (V_{DD}) is given at input terminal of the **inverter**, the PMOS becomes open circuit and NMOS will be switched OFF so the output will be pulled down to Vss. When a low-level voltage (<V_{DD}, ~0v) applied to the inverter, the NMOS will be switched OFF and PMOS will be switched ON. So, the output becomes V_{DD} or the circuit is pulled up to V_{DD}. The static CMOS inverter can used as an analog amplifier, as it has a high gain in its transition region. Next,

I_D-V_G characteristics of n-type and co-doped JLTs were measured for the devices having the dimensions of W = 5 µm, L = 5 µm, and thickness = 20 nm at low(T = 8.3 K) and high temperature(T = 300 K). Shown in Fig. 4(a)(b) and 5(a)(b). At n-type doped conditions, when the channel size kept large, it is highly expected to form several paths for electrons to flow through the channel, and these devices exhibits metallic properties, and therefore the SET functionalities are not fully analyzed. However, The inset images represents a weak n-MOSFET operation. Next, we analyzed the role of adding the boron and its compensation effect with P donors. Fig 5(a)(b), represents that the co-doping with boron doesn't show any impact. The inset images represent a weak pMOSFET operation. However, it can be also expected that, in junctionless transistors with highly-reduced dimensionality, SET functionalities re-emerge.

4. その他・特記事項(Others)

I would like to thank Prof. Kuroki, Prof. Yamada, all other staff and committee members of this training program

5. 論文・学会発表(Publication/Presentation):

None

6. 関連特許(Patent: None

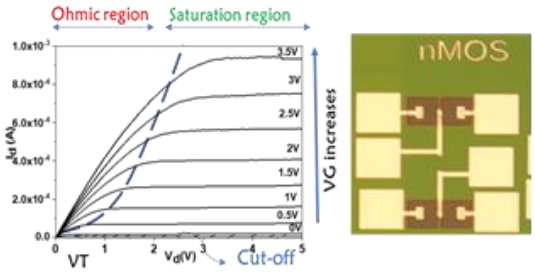

Fig.1 I-V characteristics of nMOSFET and the Fabricated device structure

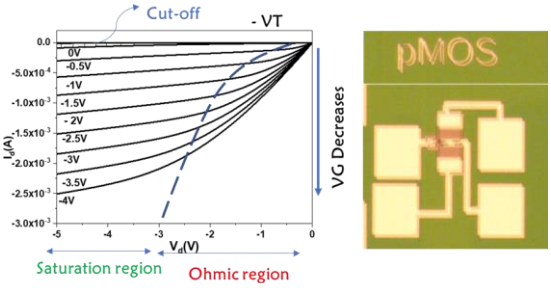

Fig.2 I-V characteristics of pMOSFET and the Fabricated device structure

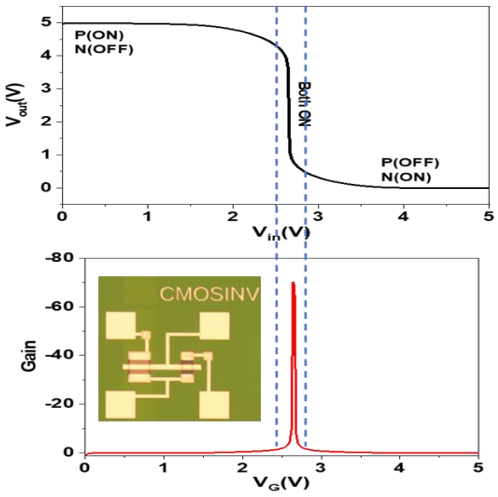

Fig.3 I-V characteristics of CMOS inverter and Fabricated device structure (Inset)

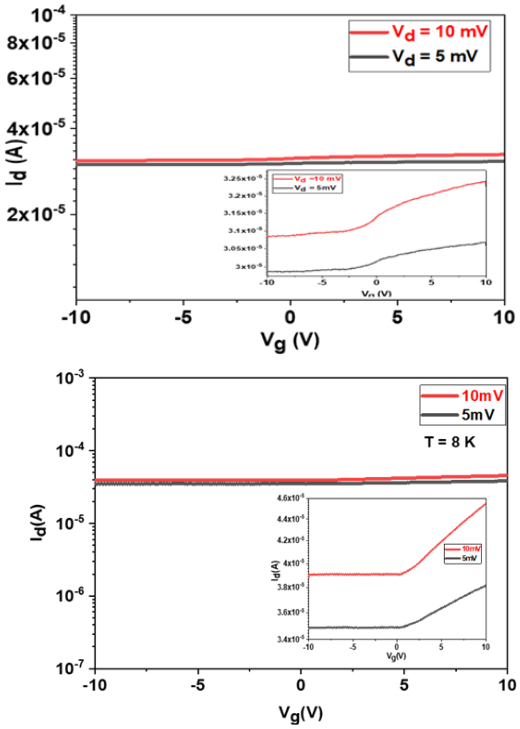

Fig.4(a) and (b) I-V characteristics of n-type doped JLTs at temperature 8.3 K and 300 K respectively

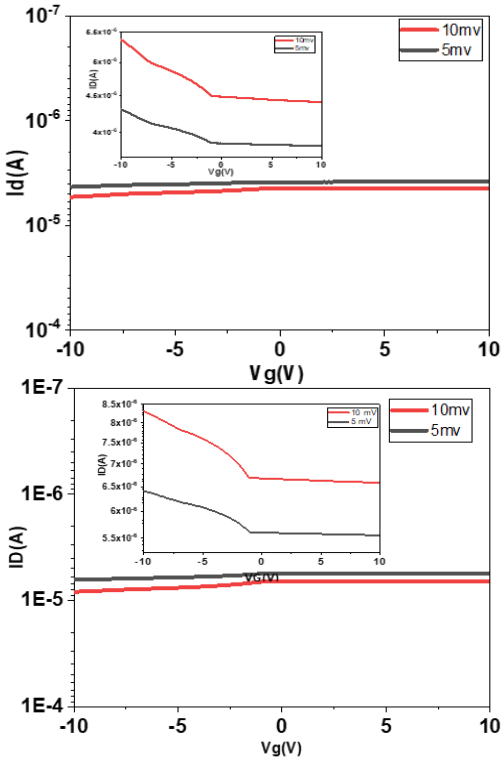

Fig.5(a) and (b) I-V characteristics of co-doped JLTs at temperature 8.3 K and 300 K respectively